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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,559	02/18/2004	Ross E. Teggatz	TI-36747	9295

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EXAMINER	
LE, LANA N	

ART UNIT	PAPER NUMBER
2614	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/781,559	TEGGATZ ET AL.	
	Examiner	Art Unit	
	Lana N. Le	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-35 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claim 10 is objected to because of the following informalities:

in claim 10, line 12, states "capacitive element for reducing reduce to operational voltage", the phrase "reduce to" seems to be inadvertently not deleted with the amendment "for reducing". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:3

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Zhou et al (herein Zhou, US 2003/0,146,815).

With respect to claim 1, Applicant's figure 1, which is prior art, disclose a load, 104; a primary component, 106 coupled to a node 112; and a secondary component array, 116, coupled to the node 112, in parallel to the primary component (Paragraph

19). Applicant's figure 1 does not disclose a reduction system intercoupled between the load and the node, the reduction system forming a voltage divider with the primary component for reducing operational voltage at the node to a target value. In the same field of endeavor, Zhou discloses a reduction system (C1, C2) intercoupled between the load (P) and the node, the reduction system forming a voltage divider with the primary component (inductance coil) for reducing operational voltage at the node to a target value (target value of 220v) (paras. 3, 27, 32; fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a reduction system in order to achieve a stable working voltage and to provide a small volume low cost device with a savings in material for an ideal resonance effect as suggested by Zhou (para. 18).

With respect to claim 2, Applicant's figure 1 shows the load being an antenna (Paragraph 19).

With respect to claims 3 and 4, AAPA disclose element number 106 is a capacitor (Paragraph 19).

With respect to claims 5 and 6, AAPA disclose element 116 is a capacitive array (Paragraph 19).

With respect to claims 8 and 9, Applicant's figure 1 discloses transistors, 122, as switchable elements (Paragraph 19).

4. Claims 10-19, 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Dautet et al (hereon Dautet; US 5,532,474).

With respect to claim 10, Applicant's figure 1, which is prior art, disclose a driver circuit, (110), instantiated within a first integrated semiconductor device; a primary resistive element (102), having a first terminal coupled the driver circuit (110), and a second terminal coupled to a first terminal of an inductive load (104);

a primary capacitive element (106), having a first terminal coupled to the node (112); and a secondary component array (116), coupled to the node (112), in parallel to the primary capacitive element (106) (Paragraph 19).

Applicant's figure 1 does not disclose a reduction system having a first terminal coupled to a second terminal of the inductive load, and having a second terminal coupled to a node; the reduction system forming a voltage divider with the primary capacitive element for reducing operational voltage at the node to a target value. In the same field of endeavor, Dautet discloses a reduction system (12, 14) having a first terminal coupled to a second terminal of a inductive load (16) and having a second terminal coupled to a node (B), the reduction system forming a voltage divider with the primary capacitive element (24) for reducing operational voltage at the node to a target value (voltage is decreased 2-3mV to target value required to trigger voltage comparator to compare with a threshold voltage) (col 6, lines 10-19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a reduction system installed in AAPA in order to provide a trigger to a voltage comparator to bring the device back to its operating voltage above the breakdown voltage as suggested by Dautet (abstract).

With respect to claims 11 and 12, AAPA figure 1 disclose the resonant structure as a radio frequency resonant circuit.

With respect to claims 13 and 14, AAPA element 102 is a resistor (Paragraph 19).

With respect to claims 15 and 16, AAPA figure 1 shows the load being an antenna (Paragraph 19).

With respect to claims 17-19, AAPA element number 106 is a capacitor (Paragraph 19).

With respect to claims 21 and 24, AAPA element 116 is a capacitive array (Paragraph 19).

With respect to claims 22 and 23, AAPA's figure 1 discloses transistors, 122, as switchable elements (Paragraph 19).

With respect to claim 25, AAPA and Dautet do not disclose the capacitor as being integrated on a semiconductor device. However, it is well known to have a capacitor integrated on a semiconductor device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate a capacitor on a semiconductor device in order to make compact and simplify the circuitry components.

With respect to claim 26, AAPA and Dautet do not disclose a transistor as being integrated on a semiconductor device. However, it is well known to have a transistor being integrated on a semiconductor device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate a transistor on a semiconductor device in order to make compact and simplify the circuitry components.

5. Claims 27 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Dautet et al (hereon Dautet; US 5,532,474) and further in view of Staker (US 4,082,999).

With respect to claims 27 and 29, AAPA and Dautet do not disclose the reduction system comprises a capacitor as a discrete component. However, Staker discloses the reduction system comprises a capacitor as a discrete component (col 2, lines 39-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the resistive voltage divider with a capactive voltage divider of Staker in order to provide an alternative type of voltage divider used for the common purpose of voltage reduction.

Regarding claim 30, AAPA, Dautet, and Staker do not disclose the capacitor is integrated in a semiconductor device. However, it is well known to integrate a capacitor in a semiconductor device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate on a semiconductor device in order to make compact and reduce size of the circuitry components.

With respect to claim 31, Applicant's figure 1, which is prior art, disclose a driver circuit (110), initiated within a first integrated semiconductor device (para. 19);

a primary resistive element (102) having a first terminal coupled the driver circuit (110) and a second terminal coupled to a first terminal of an inductive load (104);

a primary capacitive element (106) having a first terminal coupled to a node (112); providing a secondary capacitor (capacitor of 116) having a first terminal coupled to the node (112);

providing a transistor (120) having a first terminal coupled to a second terminal of the secondary capacitor (capacitor of 116), and a second terminal coupled to ground (Paragraph 19, 21). AAPA's figure 1 does not disclose a reduction system having a first terminal coupled to a second terminal of the inductive load, and having a second terminal coupled to a node; the reduction system forming a voltage divider with the primary capacitive element for reducing operational voltage at the node to a target value. In the same field of endeavor, Dautet discloses a reduction system (12, 14) having a first terminal coupled to a second terminal of a inductive load (16) and having a second terminal coupled to a node (B), the reduction system forming a voltage divider with the primary capacitive element (24) for reducing operational voltage at the node to a target value (voltage is decreased 2-3mV to target value required to trigger voltage comparator to compare with a threshold voltage) (col 6, lines 10-19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a reduction system installed in AAPA in order to provide a trigger to a voltage comparator to bring the device back to its operating voltage above the breakdown voltage as suggested by Dautet (abstract). AAPA and Dautet do not disclose the reduction system comprises one or more intercoupled capacitors. However, Staker discloses the reduction system comprises one or more capacitive voltage divider (col 2, lines 39-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the resistive voltage divider with a capactive voltage divider of Staker in order to provide an alternative type of components that make up the

voltage divider used for the common purpose of voltage reduction as suggested by Staker.

With respect to claim 32, AAPA and Dautet do not disclose providing a transistor instantiated within an integrated semiconductor device. However, it is well known to have a transistor instantiated within an integrated semiconductor device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a transistor instantiated within an integrated semiconductor device in order to make compact and simplify the circuitry components.

With respect to claim 33, AAPA and Dautet do not further disclose a transistor and the driver circuit instantiated within the first integrated semiconductor device. However, it is well known to have the transistor and driver circuit instantiated within the first integrated semiconductor device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the transistor and driver on a semiconductor device in order to make compact and simplify the circuitry components.

With respect to claim 34, AAPA and Dautet do not further disclose the capacitor instantiated within an integrated semiconductor device. However, it is well known to have a capacitor instantiated within an integrated semiconductor device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate a transistor on a semiconductor device in order to make compact and simplify the circuitry components.

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Dautet et al (hereon Dautet; US 5,532,474) in view of Zhou et al (herein Zhou, US 2003/0,146,815).

With respect to claim 28, AAPA and Dautet do not disclose the reduction system comprise a plurality of capacitors. In the same field of endeavor, Zhou discloses a reduction system comprise a plurality of capacitors (C1, C2; fig. 1; para. 3, 27). Therefore, it would be obvious to one of ordinary skill in the art to have a plurality of capacitors instead of just one capacitor in element 118 in order to provide a better impedance match and a better capacitance value.

7. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Dautet in view of Staker and further in view of Bowers et al (US 5,926,093).

With respect to claim 35, AAPA, Dautet and Staker do not disclose the secondary capacitor instantiated within the first instantaneous semiconductor device. Bowers et al teach a capacitor 18 and driver circuit 14 as being integrated on a semiconductor device as evidenced by box 10 in figure 7a. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate on a semiconductor device in order to make compact and reduce size of the circuitry components.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wuidart (U.S. 2003/0169169) disclose a tunable resonant circuit for an antenna. Humphrey (U.S. 2004/0246074) discloses a resonant filter with a capacitor array. Kennedy et al. (U.S. 2004/01202171) disclose a RF antenna with a connected resonant isolator. van Rumpt (U.S. 6,922,550) discloses a communication device with efficient excitation of a resonant circuit. Ballweber et al. (U.S. 6,889,036) disclose an integrated frequency selectable resonant coupling network. Sim (U.S. 2003/0132819) discloses an RF input stage with resonant circuits.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N. Le whose telephone number is (571) 272-7891. The examiner can normally be reached on M-F 10:00-18:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis A. Kuntz can be reached on (571) 272-7499. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lana N. Le/
Primary Examiner, Art Unit 2614